PRINCESS NORA BINT ABDULRAHMAN UNIVERSITY

College of Computer and Information Sciences

SC 302

Assignment# 5

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Due date: 15/04/2012 before 9:00 AM

Q1) Assuming a 4 KB page size, what are the logical page numbers and offsets for the following decimal address references: 4000, 16384, 14532.

Q2) Consider that the Physical memory is 128K, logical memory (per process): 32K and page size: 2K. Calculate the following values:

a) Pages per process?

b) Frames in physical memory?

c) Bits indicating page number?

d) Bits indicating offset?

Q3) Consider a simple segmentation system that has the following segment table:

Process X		
Segment #	**Base**	**Limit**
0	**3000**	**450**
1	**2000**	**350**
2	**2650**	**350**
3	**1050**	**350**

For each of the following logical addresses, determine the physical address or indicate if a segment fault occurs:

a) (0, 240) b) (2, 350) c) (1, 000)

Q4) In a demand paging system, there are 3072 bytes of physical memory and uses frame size of 1024 bytes to manage memory. The following addresses are accessed in the order specified:

2950, 476, 2050, 4023, 91, 6200, 5000, 1842, 7068, 3301

a) How many pages of memory are accessed?

b) How many frames of memory are accessed?

c) How many page faults would occur for the following replacement algorithms?

2,0,2,3,0,6,4,1,6,3

I. OPT replacement.

II. FIFO replacement.

III. LRU replacement.

Q5) A memory subsystem has a memory access time of 900 nanoseconds and a page fault time of 35 milliseconds. If the probability of a page fault is 0.2, what is the effective access time?

Q6) Suppose:

TLB lookup time = 20 ns

TLB hit ratio = 80%

Memory access time = 75 ns

a) What is the effective access time (EAT) if we assume the page fault rate is 0%?

(Show your work.) Assume the cost to update the TLB, the page table, and the

frame table (if needed) is negligible.